What is claimed is:

1. A method of regulating a supply voltage for providing a bit line voltage in a semiconductor memory device, said bit line voltage provided to memory cells in a bit line through a bit switch from said supply voltage, comprising the steps of:

detecting a bit line current provided to said memory cells; and

adjusting said supply voltage responsive to said detected bit line current to at least partially compensate for a voltage drop across said bit switch, said voltage drop being dependent at least in part on said bit line current.

2. The method of claim 1, wherein said adjusting step comprises:

increasing said supply voltage responsive to a detected increase in said bit line current and decreasing said supply voltage responsive to a detected decrease in said bit line current.

3. The method of claim 1, further comprising the step of adjusting said supply voltage to maintain a bit line voltage at said memory cells that is substantially constant during programming of said cell.

4. The method of claim 1, wherein said semiconductor memory device comprises a plurality of bit lines coupled to said supply voltage, each of said bit lines comprising respective memory cells coupled to said supply voltage through a respective bit switch, wherein a group of said memory cells are addressable together for programming,

wherein said detecting step includes the step of detecting a total bit line current provided to said plurality of bit lines, and

said adjusting step comprises the step of adjusting said supply voltage responsive to said detected total bit line current.

5. The method of claim 4, wherein said adjusting step includes increasing said supply voltage responsive to a detected increase in said total bit line current and decreasing said supply voltage responsive to a detected decrease in said total bit line current.

6. The method of claim 4,

wherein said supply voltage comprises a fixed reference voltage component and variable voltage component responsive to said detected total bit line current,

said method further comprising the step of incrementally adjusting an amount that said variable component tracks said total bit line current in response to respective memory cells from said group of memory cells reaching a programmed state.

7. The method of claim 6, wherein said amount adjusting step comprises adjusting a relationship between said variable component and said total bit line current after each respective cell from said group of memory cells reaches said programmed state.

8. The method of claim 6,

further comprising the step of generating said variable voltage component, said generating step comprising mirroring said total bit line current with a reduction ratio and generating said variable component from said mirrored portion.

9. The method of claim 8, wherein said amount adjusting step comprises the step of changing a resistance used in generating said variable voltage component.

10. The method of claim 9, wherein said changing step is responsive to a plurality of control signals indicative of whether each of said respective cells from said group of memory cells are in a programmed state.

11. The method of claim 4, wherein said semiconductor memory device is a flash memory device comprising flash memory cells organized in an array of I/O blocks, each I/O block comprising a plurality of columns and a plurality of rows, said array of I/O blocks comprising said plurality of bit lines.

12. A semiconductor memory device, comprising:

a bit line;

a plurality of memory cells and a bit switch coupled between said memory cells and a supply voltage node;

means for detecting a bit line current provided to said memory cells; and

means for adjusting a supply voltage at said supply voltage node responsive to said detected bit line current to at least partially compensate for a voltage drop across said bit switch, said voltage drop being dependent at least in part on said bit line current.

13. The semiconductor device of claim 12, wherein said adjusting means includes means for increasing said supply voltage responsive to a detected increase in said bit line current and decreasing said supply voltage responsive to a detected decrease in said bit line current.

14. The semiconductor device of claim 12, further comprising means for adjusting said supply voltage to maintain a bit line voltage at said memory cell that is substantially constant during programming of said cell.

15. The semiconductor device of claim 12, wherein said semiconductor device comprises a plurality of bit lines coupled to said supply voltage;

each of said bit lines comprising respective memory cells coupled to said supply voltage through a respective bit switch, wherein a group of said memory cells are addressable together for programming,

wherein said detecting means includes means for detecting a total bit line current provided to said plurality of bit lines, and

said adjusting means comprises means for adjusting said supply voltage responsive to said detected total bit line current.

16. The semiconductor device of claim 15, wherein said detecting means comprises a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

17. The semiconductor device of claim 15, wherein said adjusting means comprises means for increasing said supply voltage responsive to a detected increase in said bit line current and decreasing said supply voltage responsive to a detected decrease in said bit line current.

18. The semiconductor device of claim 17, wherein said adjusting means comprises:

a differential amplifier having an output coupled to said supply voltage node; and

a reference voltage generating circuit having an output coupled to a reference voltage input of said differential amplifier.

19. The semiconductor device of claim 18, wherein said reference voltage generating circuit comprises a resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

20. The semiconductor device of claim 15,

wherein said supply voltage comprises a fixed reference voltage component and variable voltage component responsive to said detected total bit line current,

said semiconductor device further comprising means for incrementally adjusting a relationship between said variable component and said total bit line current in response to respective memory cells from said group of memory cells reaching a programmed state.

21. The semiconductor device of claim 20, wherein said adjusting means comprises a reference voltage generating circuit comprising a tunable resistance circuit coupled to a current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

22. The semiconductor device of claim 21, further comprising means for adjusting a resistance of said tunable resistance circuit responsive to a plurality of control signals indicative of whether each of said respective cells from said group of memory cells is in a programmed state.

23 The semiconductor device of claim 22, wherein said amount is adjusted after each respective cell from said group of memory cells reaches said programmed state.

24. The semiconductor device of claim 20, further comprising means for generating said variable voltage component.

25. The semiconductor memory device of claim 15, wherein said semiconductor memory device is a flash memory device comprising flash memory cells organized in an array of I/O blocks, each I/O block comprising a plurality of columns and plurality of rows, said array of I/O blocks comprising said plurality of bit lines.

26. A semiconductor memory device comprising flash memory cells organized in an array comprising a plurality of columns and plurality of rows, said plurality of columns comprising a plurality of bit lines each comprising a respective one of the memory cells coupled to a supply voltage through a respective bit switch, wherein a group of said memory cells are addressable together for programming, said semiconductor device further comprising:

means for detecting a total bit line current provided to a plurality of bit lines associated with said group of memory cells;

a regulated supply voltage source for providing said supply voltage, said supply voltage comprising a fixed reference voltage component and a variable voltage component responsive to said detected total bit line current, wherein said supply voltage is adjusted to track changes in total bit line current provided to said plurality of bit lines associated with said group; and

means for adjusting, in response to respective memory cells reaching a programmed state, a relationship between said variable voltage component and said total bit line current.

27. The semiconductor device of claim 26, wherein said adjusting means comprises a reference voltage generating circuit comprising a tunable resistance circuit coupled to a

current mirror circuit, said current mirror circuit configured to mirror said total bit line current with a reduction ratio.

28. The semiconductor device of claim 27, further comprising means for adjusting a resistance of said tunable resistance circuit responsive to a control signal indicative of whether each of said respective cells are in a programmed state.

29 The semiconductor device of claim 28, wherein said amount is adjusted after each respective cell reaches said programmed state.

30. A semiconductor memory device, comprising:

a bit line;

a memory cell and a bit switch coupled between said memory cell and a supply voltage node;

a current mirror circuit configured to mirror a bit line current through said memory cell with a reduction ratio;

a voltage source having an output coupled to said supply voltage node and responsive to a reference voltage; and

a reference voltage generator circuit having an output coupled to a reference voltage input of said voltage source, said reference voltage generator circuit comprising a resistance circuit coupled to said current mirror circuit,

wherein said reference voltage generator circuit provides a reference voltage for said voltage source that is responsive to said mirrored bit line current,

whereby said supply voltage at said supply voltage node is adjusted responsive to said bit line current to at least partially compensate for a voltage drop across said bit switch, said voltage drop being dependent at least in part on said bit line current.